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UNITED STATES PATENT AND TRADEMARK OFFICE

BEFORE THE BOARD OF PATENT APPEALS
AND INTERFERENCES

Ex parte ZAHI SAID ABUHAMDEH and PHILIP J. PEARS

Appeal 2008-4138
Application 10/647,018
Technology Center 2100

Decided:[1] March 18, 2009

Before JOSEPH L. DIXON, JAY P. LUCAS, and
THU A. DANG, *Administrative Patent Judges.*

DANG, *Administrative Patent Judge.*

DECISION ON APPEAL

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[1] The two-month time period for filing an appeal or commencing a civil action, as recited in 37 C.F.R. § 1.304, begins to run from the decided date shown on this page of the decision. The time period does not run from the Mail Date (paper delivery) or Notification Date (electronic delivery).

I. STATEMENT OF THE CASE

Appellants appeal under 35 U.S.C. § 134(a) from a final rejection of claims 1-20. We have jurisdiction under 35 U.S.C. § 6(b).

A. INVENTION

According to Appellants, the invention relates generally to testing integrated circuits, and more particularly, relates to an on-chip implementation of Joint Test Action Group (JTAG) master which can affect a plurality of predefined tests of the chip without regard to other devices on the same circuit board (Spec. 1, ll. 6-10).

B. ILLUSTRATIVE CLAIM

Claim 1 is exemplary and is reproduced below:

1. An integrated circuit chip, comprising:

a) core logic;

b) an on-chip JTAG TAP coupled to said core logic;

c) an on-chip JTAG master coupled to said JTAG TAP; and

d) an on-chip mircroprocessor interface coupled to said JTAG master.

C. REJECTIONS

The prior art relied upon by the Examiner in rejecting the claims on appeal is:

Texas Instruments, SN54LVT8980, SN74LVT8980 EMBEDDED TEST-BUS CONTROLLERS, (1996) (hereinafter "Texas Instruments").

Patavalis, *A Brief Introduction to the JTAG Boundary Scan Interface*, inAccess (2001) (hereinafter "Patavalis").

Claims 1-20 stand rejected under 35 U.S.C. § 103(a) over the teachings of Texas Instruments in view of Patavalis.

We affirm.

II. ISSUE

Have Appellants shown that the Examiner erred in finding that claims 1-20 are unpatentable under 35 U.S.C. § 103(a)? In particular, the issue turns on whether the combination of Texas Instruments and Patavalis teaches and/or would have suggested "[a]n integrated circuit chip" which comprises "an on-chip JTAG TAP coupled to said core logic" and "an on-chip JTAG master coupled to said JTAG TAP" (claim 1).

III. FINDINGS OF FACT

The following Findings of Fact (FF) are shown by a preponderance of the evidence.

Texas Instruments

1. Texas Instruments discloses testability integrated circuits comprising embedded test-bus controllers (eTBC) to master JPTG test access port (TAP) under the command of an embedded host microprocessor (p. 1, "description").
2. The microprocessor interface is coupled to the eTBC which sources/receives JPTG TAP signals TCK, TMS, TDO, TDI to/from the target (p. 5, Fig. 1).
3. In Texas Instruments, the eTBC can fully support multidrop backplane TAP configurations, implemented with TI's addressable scan ports (ASP) coupled to the eTBC (pp. 6-9, Figs. 3-5).
4. The configuration can be a multidrop TAP configuration in a passive-backplane application implemented with a test-control architecture, a passive-backplane application implemented with a distributed test-control architecture, or a multidrop TAP configuration in an active-backplane application (*id.*), wherein the ASP port associated with TAP signals TCK, TMS, TDO, TDI may be located in the same module as the microprocessor and eTBC (pp. 7-8, Figs. 3-4).

Patavalis

5. Patavalis discloses a JTAG Boundary Scan Interface Architecture, wherein the integrated circuit chip comprises a core logic and an on-chip JTAG TAP coupled to the core logic, wherein on-chip test

interface is provided with TAP signals TCK, TMS, TDI and TDO and is controlled by the JTAG TAP controller (pp. 2-3; Fig. 1).

IV. PRINCIPLES OF LAW

"[T]he PTO gives claims their 'broadest reasonable interpretation.'" *In re Bigio*, 381 F.3d 1320, 1324 (Fed. Cir. 2004) (quoting *In re Hyatt*, 211 F.3d 1367, 1372 (Fed. Cir. 2000)). "Moreover, limitations are not to be read into the claims from the specification." *In re Van Geuns*, 988 F.2d 1181, 1184 (Fed. Cir. 1993) (citing *In re Zletz*, 893 F.2d 319, 321 (Fed. Cir. 1989)). Our reviewing court has repeatedly warned against confining the claims to specific embodiments described in the specification. *Phillips v. AWH Corp.*, 415 F.3d 1303, 1323 (Fed. Cir. 2005) (en banc).

> Section 103 forbids issuance of a patent when "the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains."

KSR Int'l Co. v. Teleflex Inc., 127 S. Ct. 1727, 1734 (2007).

In *KSR*, the Supreme Court emphasized "the need for caution in granting a patent based on the combination of elements found in the prior art," and discussed circumstances in which a patent might be determined to be obvious. *Id.* at 1739 (citing *Graham v. John Deere Co.*, 383 U.S. 1, 12 (1966)). The Court reaffirmed principles based on its precedent that "[t]he combination of familiar elements according to known methods is likely to be obvious when it does no more than yield predictable results." *Id.* The Court

noted that "[c]ommon sense teaches . . . that familiar items may have obvious uses beyond their primary purposes, and in many cases a person of ordinary skill will be able to fit the teachings of multiple patents together like pieces of a puzzle." *Id.* at 1742. "A person of ordinary skill is also a person of ordinary creativity, not an automaton." *Id.*

The Federal Circuit recognized that "[a]n obviousness determination is not the result of a rigid formula disassociated from the consideration of the facts of a case. Indeed, the common sense of those skilled in the art demonstrates why some combinations would have been obvious where others would not." *Leapfrog Enters., Inc. v. Fisher-Price, Inc.*, 485 F.3d 1157, 1161 (Fed. Cir. 2007) (citing *KSR*, 127 S. Ct. at 1739). The Federal Circuit relied in part on the fact that Leapfrog had presented no evidence that the inclusion of a reader in the combined device was "uniquely challenging or difficult for one of ordinary skill in the art" or "represented an unobvious step over the prior art." *Id.* at 1162 (citing *KSR*, 127 S. Ct. at 1741).

To address obviousness questions involving combinations of known elements, the Supreme Court explains:

> When a work is available in one field of endeavor, design incentives and other market forces can prompt variations of it, either in the same field or a different one. If a person of ordinary skill can implement a predictable variation, § 103 likely bars its patentability. For the same reason, if a technique has been used to improve one device, and a person of ordinary skill in the art would recognize that it would improve similar devices in the same way, using the technique is obvious unless its actual application is beyond his or her skill. *Sakraida* [*v. AG Pro, Inc.*, 425 U.S. 273 (1976)] and *Anderson's-Black Rock*[,

> *Inc. v. Pavement Salvage Co.*, 396 U.S. 57 (1969)] are illustrative—a court must ask whether the improvement is more than the predictable use of prior art elements according to their established functions.

KSR, 127 S. Ct. at 1740.

V. ANALYSIS

Claim 1

Appellants contend that "[t]hroughout the specification it is made clear that the invention is directed to a single chip which contains multiple JTAG components," that "[t]he preamble of claim 1 is directed to 'an integrated circuit chip'," and that "[a]ll of the JTAP components are described in the claim as 'on-chip'" (App. Br. 12). Thus, Appellants argue that, as correctly summarized in the Final Rejection, "although the prior art shows all of the elements of claim1, they are not all on the same chip" (*Id.*).

However, the Examiner finds that

> [i]t would have [been] obvious to one having ordinary skill in the art to combine a JTAG TAP and JTAG master to be on the same chip with the core logic as a JTAG master (eTBC) can master all TAP signals required to support one 4-or 5-wire IEEE Std 1149.1 serial test bus – test clock (TCK), test mode select (TMS), test data input (TDI), test data output (TDO), and test reset (TRST) directly under full control of the microprocessor/microcontroller host without need for additional logic or buffering and achieve the predictable results of reducing signal processing time.

(Ans. 7-8).

Thus, the issue we address on appeal is whether the combination of Texas Instruments and Patavalis teaches and/or would have suggested "[a]n integrated circuit chip" which comprises "an on-chip JTAG TAP coupled to said core logic" and "an on-chip JTAG master coupled to said JTAG TAP" (Claim 1).

We give the claims their broadest reasonable interpretation. *See In re Bigio,* 381 F.3d at 1324. Furthermore, our analysis will not read limitations into the claims from the specification. *See In re Van Geuns,* 988 F.2d at 1184.

Appellants' arguments that "the invention is directed to a single chip" and that the prior art does not show the claimed elements "all on the same chip" (App. Br. 12) are not commensurate with the express language of claimed invention. That is, claim 1 does not recite any such "single chip" or "same chip" limitation, and thus, we will not read such limitations into independent claim 1.

Independent claim 1 simply does not place any specific context or restriction on what the term "comprising" in "[a]n integrated circuit chip, comprising" or the term "on-chip" in "on-chip JTAG TAP," "on-chip JTAG master" and "on-chip microprocessor" is to be, is to represent, or is to mean, other than integrated circuit chip "comprising" the claimed elements, and that the "JTAG TAP" is "on-chip," the "JTAG master" is "on-chip," and the "microprocessor" is "on-chip" (claim 1). Thus, the terminology "integrated circuit chip, comprising" and "on-chip" cannot be confined to a specific

disclosed embodiment when independent claim 1 does not recite a specific limitation that correspond to a specific embodiment.

The language of claim 1 does not distinguish the "integrated circuit chip, comprising" the claimed elements from and interpretation where an integrated circuit which includes the claimed elements, connected yet provided at different locations. Furthermore, the language of claim 1 does not distinguish the "on-chip" JTAG TAP, "on-chip" JTAG master, and the "on-chip" microprocessor from an on-chip JTAG TAP provided on one chip connected to an on-chip JTAG master provided on another chip that is connected to an on-chip microprocessor provided on yet another chip.

We also note that such label "integrated circuit" or "on-chip" does not change the functionality of or provide any additional function to the claimed chip, but rather, is merely a label set forth for the chip or the JTAG TAP, JTAG master and microprocessor. In fact, we find that such "JTAG" and "JTAG TAP" terms are also labels set forth for the master and the port that do not provide any function. Such labels do not distinguish the claimed invention from the prior art in terms of obviousness.

Texas Instruments discloses an integrated circuit chip comprising an eTBC coupled to a JTAG TAP and an embedded host microprocessor (FF 1-2). We find the eTBC to be a JTAG master wherein the integrated circuit chip of Texas Instrument comprises the on-chip JTAG master coupled to a JTAG TAP, and an on-chip microprocessor interface coupled to the JTAG master.

Furthermore, Texas Instruments discloses an addressable scan port (ASP) coupled to the eTBC that is associated with TAP signals TCK, TMS, TDO, TDI, wherein the ASP port may be located in the same module as the microprocessor and eTBC (FF 3-4). We find the ASP port coupled to the eTBC to be an on-chip JTAG TAP port coupled to the on-chip JTAG master.

Patavalis discloses an integrated circuit chip comprising core logic and an on-chip JTAG TAP coupled to the core logic (FF 5). We find that an artisan would have understood Texas Instruments, when combined with Patavalis, to teach and strongly suggest "an integrated circuit chip" which comprises "an on-chip JTAG TAP coupled to said core logic" and "an on-chip JTAG master coupled to said JTAG TAP." In fact, as the Appellants admit, "the prior art shows all of the elements" of claim 1 (App. Br. 12).

Though Appellants contend that "[t]he Examiner did not state where that alleged incentive could be found [to combine the references]" (App. Br. 11), to address the issue of obviousness, we will determine whether the subject matter sought to be patented by Appellants as a whole would have been obvious to the artisan as we consider the facts of the case and the common sense of those skilled in the art. *See Leapfrog*, 485 F.3d at 1161. That is, "obviousness determination is not the result of a rigid formula disassociated from the consideration of the facts of a case." *Id.* The test for obviousness is rather what the combined teachings of the references would have suggested to those of ordinary skill in the art. *See In re Keller*, 642 F.2d at 425 and *In re Young*, 927 F.2d 588, 591 (Fed. Cir. 1991).

Appellants have presented no evidence that adding the teachings of Patavalis of placing the JTAG TAP coupled to the core logic on the integrated circuit chip of Texas Instruments "was uniquely challenging or difficult for one of ordinary skill in the art" (*see Leapfrog*, 485 F.3d at 1162), nor have Appellants presented evidence that these "represented an unobvious step over the prior art" (*id.*). Rather, Appellants' invention is simply an arrangement of the well-known teachings of a JTAG TAP on the well-known teaching of an integrated circuit chip. In fact, as set forth in Texas Instruments, it is well-known to provide a TAP port coupled to a module comprising a JTAG master and a microprocessor embedded within (FF 3), wherein various architectures are available including an architecture with the TAP port integrated on the same module as the JTAG master and microprocessor (FF 4).

We find that a person of ordinary skill would have been able at the time of the invention to fit the teachings of Texas Instruments and Patavalis together like pieces of a puzzle to master TAP signals "under full control of the microprocessor/microcontroller host without need for additional logic or buffering and achieve the predictable results of reducing signal processing time" as set forth by the Examiner (Ans. 8), since the person of ordinary skill is also a person of ordinary creativity, not an automaton. The combined teachings of the references represent merely a combination of familiar elements according to known methods and do no more than yield predictable results. *See KSR,* 127 S. Ct. at 1739. That is, the invention is no more than the predictable use of prior art elements according to their established

functions. *See id.* at 1740. A person having ordinary skill in the art uses these known integrated circuit chip components for their intended purpose. *See Anderson's-Black Rock, Inc. v. Pavement Salvage Co.*, 396 U.S. 57.

Further, even if independent claim 1 were to require that these integrated circuit chip components be contained in a "single chip," putting these components in a single chip appears to be no more than a simple arrangement of old elements, with each performing the same function it had been known to perform, yielding no more than one would expect from such an arrangement, and thus prima facie obvious. *See KSR*, 127 S. Ct. at 1740.

Accordingly, we conclude that Appellants' arguments are unpersuasive in overcoming a final conclusion of obviousness, of the subject matter as a whole of claim 1, given the strength of the Examiner's prima facie obviousness showing based on the teachings of Texas Instruments in view of Patavalis. Thus, we conclude that the Appellants have not shown that the Examiner erred in rejecting claim 1 under 35 U.S.C. § 103(a).

Claims 2, 3, 5, 6, 9-15, 19, and 20

As to claims 2, 3, 5, 6, 9-15, 19, and 20, Appellants do not provide separate arguments from those of claim 1. In particular, Appellants argue that the elements in the prior art are "on a separate chip" not on the "same" or "single" chip (App. Br. 14, 19) or "requires three chips" (App. Br. 18, 21). As discussed above regarding claim 1, such "same" or "single" limitation is not recited in the claims. We find that Texas Instruments in view of Patavalis teaches and/or would have suggested the claimed

limitations. Accordingly, we conclude that the Appellants have not shown that the Examiner erred in rejecting claims 2, 3, 5, 6, 9-15, 19, and 20 as unpatentable over Texas Instruments in view of Patavalis under 35 U.S.C. § 103(a).

Claims 4, 7, 8, and 16-18

As to claims 4, 7, 8, and 16-18, Appellants argue that the Examiner "fail[s]to recite all of the claimed limitations" (App. Br. 15). However, the Examiner finds that Texas Instruments in view of Patavalis teaches and/or suggests such limitations (Ans. 4-6, 9, 11-13, and 18-19). No evidence has been presented by the Appellants that is contrary to the Examiner's finding. Accordingly, we conclude that Appellants have not shown that the Examiner erred in rejecting claims 4, 7, 8, and 16-18 as unpatentable over Texas Instruments in view of Patavalis under 35 U.S.C. § 103(a).

VI. CONCLUSION OF LAW

(1) Appellants have not shown that the Examiner erred in concluding that claims 1-20 are unpatentable under 35 U.S.C. § 103(a) over the teachings of Texas Instruments and Patavalis.

(2) Claims 1-20 are not patentable.

VII. DECISION

We affirm the Examiner's rejection of claims 1-20 under 35 U.S.C. § 103(a).

No time period for taking any subsequent action in connection with this appeal may be extended under 37 C.F.R. § 1.136(a).

AFFIRMED

rwk

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